PATENT
Docket No. 333772000101

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Ararat Kapouytian

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Akihiko ITO, et al.

Serial No.: To Be Assigned

Filing Date: Herewith

For: SEMICONDUCTOR DEVICE TESTING APPARATUS AND A TEST TRAY FOR USE IN THE TESTING APPARATUS

Examiner: To Be Assigned

Group Art Unit: To Be Assigned

09664744 - 092501

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Dear Sir:

Prior to examination on the merits, please amend this application as follows.

AMENDMENTS

In the Specification:

On page 1, line 3, before the section entitled the "TECHNICAL FIELD", please insert the following paragraph:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Application Serial No. 09/254,084, entitled "Semiconductor Device Testing Apparatus and a Test Tray for Use in the Testing Apparatus", and filed on February 26, 1999.--

Please replace the paragraph beginning at page 1, line 5 with the following rewritten paragraph:

--The present invention relates to a semiconductor device testing apparatus suitable for testing semiconductor integrated circuit elements which are typical of semiconductor devices, and more particularly to a semiconductor device testing apparatus of the type in which semiconductor devices are transported to a testing section or test section where they are tested for their electrical characteristics, followed by being carried out of the test section and then being sorted out into conforming articles and non-conforming articles on the basis of the test results, and to a test tray for use in the IC tester in which the tray is moved in a circulating manner along a predetermined path of transport.--

Please replace the paragraph beginning at page 1, line 18 (and ending on page 2, line 10) with the following rewritten paragraph:

--Many semiconductor device testing apparatuses (commonly called IC tester) for measuring the electrical characteristics of semiconductor devices to be tested (commonly called DUT (device under test)) by applying a signal of a predetermined test pattern to the devices have a semiconductor transporting and handling (processing) apparatus (commonly called handler) integrally incorporated therein for transporting semiconductor devices to a testing section where they are brought into electrical contact with device sockets on the tester head of the testing apparatus (a component of the testing apparatus for supplying and receiving various electrical signals for testing purposes), followed by carrying the tested semiconductor devices out of the testing section and sorting them out into conforming and non-conforming articles on the basis of the test results. The semiconductor device testing apparatus having integrated therein the handler of the type described above is herein termed simply "IC tester". In the following disclosure the present invention will be described by taking semiconductor integrated circuit elements (which will be referred to as IC hereinafter) which are typical of semiconductor devices by example for the convenience of explanation.--

Please replace the paragraph beginning at page 2, line 11 with the following rewritten paragraph:

--First, the general construction of one example of the prior art semiconductor device testing apparatus (which will be referred to as IC tester hereinafter) will be described with reference to Fig. 11.--

Please replace the paragraph beginning at page 11, line 7 with the following rewritten paragraph:

--The sorting operation in the unloader section 8 will now be described. In the IC tester shown in Fig. 11, the operation of sorting and transshipping tested ICs is performed with respect to only universal trays arranged adjacent to each of the first and second positions A and B. Specifically, arranged at the first position A are universal trays la and lb. It is assumed that classification categories 1 and 2 are assigned to the universal trays la and lb, respectively. While the test tray 3 is stopped at the first position A, only the tested ICs belonging to the categories 1 and 2 are picked up from the test tray and transferred onto the corresponding universal trays la and lb, respectively. Once the test tray 3 stopping at the first position A has been depleted of the ICs belonging to the categories 1 and 2, the test tray is moved to the second position B.--

Please replace the paragraph beginning at page 13, line 25 (and ending on page 14, line 7) with the following rewritten paragraph:

--The IC carrier 34 holds an IC in place with its leads or pins PN exposed downwardly as shown in Fig. 13. The tester head 100 is provided with an IC socket having contacts 101 extending upwardly from the top surface thereof. The exposed pins PN of the IC are urged against the contacts 101 of the IC socket to establish electrical connection between the IC and the socket. To this end, a pusher 103 for pushing and holding an IC down is mounted above the tester head and is configured to push the IC accommodated in an IC carrier 34 from above to bring the pins PN into contact with the tester head.--

Please replace the paragraph beginning at page 17, line 5 with the following rewritten paragraph:

--In testing ICs in the testing section 42, a relatively long time required per test necessitates a corresponding long waiting time until an IC carried into the soak chamber 41 as loaded on a test tray comes up for testing in the testing section 42, meaning that the test tray transporting mechanism need not be so fast in operation. In addition, the number of test trays to be stacked in the soak chamber 41 can be reduced.--

Please replace the paragraph beginning at page 17, line 12 with the following rewritten paragraph:

--This, however, requires a very long time to go through the test on all of the ICS, leading to a poor utilization ratio of the expensive IC tester and hence the serious disadvantage that the testing cost per IC is greatly increased.--

Please replace the paragraph beginning at page 17, line 23 (and ending on page 18, line 5) with the following rewritten paragraph:

--In addition, an increase in simultaneous measurement throughput in number of ICs for simultaneous measurement would require an increase in the number of ICs which can be handled by the transporting and handling mechanism including the X-Y transports 71 and 81 for the loader section 7 and the unloader section 8, respectively. While the throughput in number of ICs depends on the performance or throughput capacity of this transporting and handling mechanism, in the case that the testing time is relatively long, there would be no particular problem if the throughput in number of ICs was not increased so much.--

Please replace the paragraph beginning at page 18, line 14 with the following rewritten paragraph:

--However, although it would not take much cost to make the speed of operation of the test tray transporting mechanism of only limited extent, it would require substantial cost to increase the operation speed to nearly the maximal limit, providing the disadvantage of rendering the initial cost of the entire IC tester very expensive. On top of that, in order to transport test trays at high speed, it is required to increase the throughput in number of ICs of the transporting and handling mechanism including the X-Y transports 71 and 81. Not only is it costly to increase the throughput in number of ICs, but also there is naturally a limit to increasing the throughput in

number of ICs. It should also be noted that when the testing time in the testing section 42 is relatively short, increasing the simultaneous measurement throughput in number of ICs would not lead to a significant enhancement of efficiency.--

Please replace the paragraph beginning at page 19, line 3 with the following rewritten paragraph:

--A first object of the present invention is to provide an IC tester which is capable of reducing the time required to complete testing on all of the ICs to thereby enhance the utilization ratio.--

Please replace the paragraph beginning at page 19, line 10 with the following rewritten paragraph:

--A third object of the present invention is to provide an IC tester which provides an increased throughput in number of ICs through the loader and unloader sections to thereby shorten the time required to complete testing on all of the ICs to be tested.--

Please replace the paragraph beginning at page 43, line 11 with the following rewritten paragraph:

--The vertical transport mechanism is at rest in operation until two test trays are transported onto the lowermost stage. Once two test trays have been transported from the testing section 42 onto the lowermost stage of the vertical transport mechanism, the vertical transport mechanism is actuated to move the test trays on the successive stages upwardly by one stage in the vertical direction. While two test trays on the lowermost stage are moved up to the uppermost stage by the upward movement of the successive stages by actuation of the vertical transport mechanism, the tested ICs are relieved of either heat or cold to be restored to the outside temperature (room temperature).--

Please replace the paragraph beginning at page 94, line 20 (and ending on page 95, line 19) with the following rewritten paragraph:

--In the fifth embodiment described above, the depth of the constant temperature chamber 4 is expanded by a dimension corresponding approximately to one transverse width (length of the

minor edge) of the rectangular test tray 3 and two paths of transport for test trays are provided for the section of path extending from the soak chamber 41 to the testing section 42 so that two test trays may be substantially simultaneously transported along the respective transport paths independently of each other, or alternatively the width of the test tray transport path for the section extending from the soak chamber 41 to the testing section 42 is broadened to be approximately equal to the sum of transverse widths of two test trays so that two test trays in an integrally joined state may be simultaneously transported. However, in the case that the time required per test in the testing section 42 is relatively short, it is preferable that with the construction of the test tray transport path extending from the loader section 7 through the soak chamber 41 and the testing section 42 of the constant temperature chamber 4 to the exit chamber 5 being retained as in the illustrated prior art IC tester, the depth (length in the Y-axis direction) of the loader section 7 and the unloader section 8 be expanded by a dimension corresponding approximately to one transverse width (length of the minor edge) of the rectangular test tray 3, and two test tray transport paths are provided for the section of path extending from the unloader section 8 to the loader section 7 so that two test trays may be substantially simultaneously transported along the respective transport paths independently of each other.--

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 333772000101.

Respectfully submitted,

Dated: September 25, 2001 By: Ararat Kapouytian

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph beginning at page 1, line 5 has been amended as follows:

The present invention relates to a semiconductor device testing apparatus suitable for testing semiconductor integrated circuit elements which are typical of semiconductor devices, and more particularly to a semiconductor device testing apparatus of the type in which semiconductor devices are transported to a testing section or test section where they are tested for their electrical characteristics, followed by being carried out of the test section and then being sorted out into conforming articles and non-conforming articles on the basis of the test results, and to a test tray for use in the IC tester in which [a]the tray is moved in a circulating manner along a predetermined path of transport.

The paragraph beginning at page 1, line 18 (and ending on page 2, line 10) has been amended as follows:

Many [of]semiconductor device testing apparatuses (commonly called IC tester) for measuring the electrical characteristics of semiconductor devices to be tested (commonly called DUT (device under test)) by applying a signal of a predetermined test pattern to the devices have a semiconductor transporting and handling (processing) apparatus (commonly called handler) integrally incorporated therein for transporting semiconductor devices to a testing section where they are brought into electrical contact with device sockets on the tester head of the testing apparatus (a component of the testing apparatus for supplying and receiving various electrical signals for testing purposes), followed by carrying the tested semiconductor devices out of the testing section and sorting them out into conforming and non-conforming articles on the basis of the test results. The semiconductor device testing apparatus having integrated therein the handler of the type described above is herein termed simply "IC tester". In the following disclosure the present invention will be described by taking semiconductor integrated circuit elements (which will be referred to as IC hereinafter) which are typical of semiconductor devices by example for the convenience of explanation.

The paragraph beginning at page 2, line 11 has been amended as follows:

First, the general construction of one example of the prior art semiconductor device testing apparatus (which will be referred to as IC tester hereinafter) will be described with reference to Fig. 11.

The paragraph beginning at page 11, line 7 has been amended as follows:

The sorting operation in the unloader section 8 will now be described. In the IC tester shown in Fig. 11, the operation of sorting and transshipping tested ICs is performed with respect to only universal trays arranged adjacent to each of the first and second positions A and B. Specifically, arranged at the first position A are universal trays la and lb. [Let it assume]It is assumed that classification categories 1 and 2 are assigned to the universal trays la and lb, respectively[, while]. While the test tray 3 is stopped at the first position A, only the tested ICs belonging to the categories 1 and 2 are picked up from the test tray and transferred onto the corresponding universal trays la and lb, respectively. Once the test tray 3 stopping at the first position A has been depleted of the ICs belonging to the categories 1 and 2, the test tray is moved to the second position B.

The paragraph beginning at page 13, line 25 (and ending on page 14, line 7) has been amended as follows:

The IC carrier 34 holds an [18]IC in place with its leads or pins PN exposed downwardly as shown in Fig. 13. The tester head 100 is provided with an IC socket having contacts 101 extending upwardly from the top surface thereof. The exposed pins PN of the IC are urged against the contacts 101 of the IC socket to establish electrical connection between the IC and the socket. To this end, a pusher 103 for pushing and holding an IC down is mounted above the tester head and is configured to push the IC accommodated in an IC carrier 34 from above to bring the pins PN into contact with the tester head.

The paragraph beginning at page 17, line 5 has been amended as follows:

In testing ICs in the testing section 42, a relatively long time required per [a]test necessitates a corresponding long waiting time until an IC carried into the soak chamber 41 as loaded on a test tray comes up for testing in the testing section 42, meaning that the test tray

transporting mechanism need not be so fast in operation. In addition, the number of test trays to be stacked in the soak chamber 41 can be reduced.

The paragraph beginning at page 17, line 12 has been amended as follows:

This, however, requires a very long time to go through the test on all of the ICS, leading to a poor utilization ratio of the expensive IC tester and hence the serious disadvantage that the testing cost per [an]IC is greatly [an]increased.

The paragraph beginning at page 17, line 23 (and ending on page 18, line 5) has been amended as follows:

In addition, an increase in simultaneous measurement throughput in number of ICs [in number of ICs]for simultaneous measurement would require an increase in the number of ICs which can be handled by the transporting and handling mechanism including the X-Y transports 71 and 81 for the loader section 7 and the unloader section 8, respectively. While the throughput in number of ICs depends on the performance or throughput capacity of this transporting and handling mechanism, in the case that the testing time is relatively long, there would be no particular problem if the throughput in number of ICs was not increased so much.

The paragraph beginning at page 18, line 14 has been amended as follows:

However, although it would not take much cost to make the speed of operation of the test tray transporting mechanism of only [to a]limited extent, it would require substantial cost to increase the operation speed to nearly the maximal limit, providing the disadvantage of rendering [he]the initial cost of the entire IC tester very expensive. On top of that, in order to transport test trays at high speed, it is required to increase the throughput in number of ICs of the transporting and handling mechanism including the X-Y transports 71 and 81. Not only is it costly to increase the throughput in number of ICs, but also[is] there is naturally a limit to increasing the throughput in number of ICs. It should also be noted that when the testing time in the testing section 42 is relatively short, increasing the simultaneous measurement throughput in number of ICs would not lead to a significant enhancement of efficiency.

The paragraph beginning at page 19, line 3 has been amended as follows:

A first object of the present invention is to provide an IC tester which is capable of reducing the time required [before completion of]to complete testing on all of the ICs to thereby enhance the utilization ratio.

The paragraph beginning at page 19, line 10 has been amended as follows:

A third object of the present invention is to provide an IC tester which provides an increased throughput in number of ICs through the loader and unloader sections to thereby shorten the time required [before completion of]to complete testing on all of the ICs to be tested.

The paragraph beginning at page 43, line 11 has been amended as follows:

The vertical transport mechanism is at rest in operation until two test trays are transported onto the lowermost stage. Once two test trays [has]have been transported from the testing section 42 onto the lowermost stage of the vertical transport mechanism, the vertical transport mechanism is actuated to move the test trays on the successive stages upwardly by one stage in the vertical direction. While two test trays on the lowermost stage are moved up to the uppermost stage by the upward movement of the successive stages by actuation of the vertical transport mechanism, the tested ICs are relieved of either heat or cold to be restored to the outside temperature (room temperature).

The paragraph beginning at page 94, line 20 (and ending on page 95, line 19) has been amended as follows:

In the fifth embodiment described above, the depth of the constant temperature chamber 4 is expanded by a dimension corresponding approximately to one transverse width (length of the minor edge) of the rectangular test tray 3 and two paths of transport for test trays are provided for the section of path extending from the soak chamber 41 to the testing section 42 so that two test trays may be substantially simultaneously transported along the respective transport paths independently of each other, or alternatively the width of the test tray transport path for the section extending from the soak chamber 41 to the testing section 42 is broadened to be approximately equal to the sum of transverse widths of two test trays so that two test trays in an integrally joined state may be simultaneously transported. However, in the case that the time required per test in the testing section 42 is relatively short, it is preferable that with the

construction of the test tray transport path extending from the loader section 7 through the soak chamber 41 and the testing section 42 of the constant temperature chamber 4 to the exit chamber 5 being retained as in the illustrated prior art IC tester, the depth (length in the Y-axis direction) of the loader section 7 and the unloader section 8 be expanded by a dimension corresponding approximately to one transverse width (length of the minor edge) of the rectangular test tray 3, and two test tray transport paths are provided for the section of [oath]path extending from the unloader section 8 to the loader section 7 so that two test trays may be substantially simultaneously transported along the respective transport paths independently of each other.

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